Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Canceled)

3. (Currently amended) The method of claim [11]] 23, wherein said oxidation-resistant film is a silicon nitride film.

4. (Withdrawn) A method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate, comprising the steps of:

forming a first silicon (Si) layer on the semiconductor substrate;

selectively etching said first Si layer formed on a region where the gate insulating film of said MOS transistor is to be formed, thereby removing it;

covering an entire surface of the semiconductor substrate, inclusive of a side of said first Si layer exposed by the selective etching, with an oxidation-resistant film;

selectively removing said oxidation-resistant film on a region where the gate insulating film of said MOS transistor is to be formed and selectively removing said oxidation-resistant film on a region where the floating gate of said non-volatile memory transistor is to be formed;

forming the oxide film by thermal oxidation on the region where said floating gate is to be formed and forming the gate insulating film on a region where said MOS transistor is to be formed;

removing the remaining oxidation-resistant film;

removing the remaining first Si layer using said oxide film as a mask, thereby forming the floating gate of said non-volatile memory cell transistor;

forming a tunneling insulating film of said non-volatile memory cell on the entire surface of the semiconductor substrate inclusive of the surface of the gate insulating film on the region where said MOS transistor is to be formed;

forming a second Si layer on the entire surface of said semiconductor substrate; and

selectively etching said second Si layer so that the control gate of said non-volatile memory cell and the gate of said MOS transistor are simultaneously formed.

5. (Withdrawn) A method of manufacturing a semiconductor device according to claim 4, further comprising the step of selectively removing said tunneling insulating film formed on the gate insulating film on the region where said MOS transistor is to be formed.

6. (Withdrawn) A method of manufacturing a semiconductor device according to claim 4 or 5, wherein said oxidation-resistant film is a silicon nitride film.

7. (Withdrawn) A method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate, said method comprising the steps of:

forming a first silicon (Si) layer on the semiconductor substrate;

forming an oxidation-resistant oxide film on said first Si layer;

selectively removing the oxidation-resistant film on a region where said floating gate is to be formed;

selectively etching said first Si layer of said MOS transistor on a region where a gate insulating film is to be formed, thereby removing it;

forming the oxide film by thermal oxidation on the region where the floating gate is to be formed, the gate insulating film on the region where said MOS transistor is to be formed and an

oxide film piece on the side of said first Si layer;

removing the remaining oxidation-resistant film;

removing said remaining first Si layer using said oxide film as a mask, thereby forming the floating gate of said non-volatile memory cell transistor;

forming a tunneling insulating film of said non-volatile memory cell on the entire surface of the semiconductor substrate inclusive of the surface of the gate insulating film on the region where said MOS transistor is to be formed;

forming a second Si layer on the entire surface of said semiconductor substrate; and

selectively etching said second Si layer so that the control gate of said non-volatile memory cell and the gate of said MOS transistor are simultaneously formed.

8. (Withdrawn) A method of manufacturing a semiconductor device according to claim 7, wherein a gate of said MOS transistor is formed to cover said oxide film piece.

9. (Withdrawn) A method of manufacturing a semiconductor device according to claim 7, further comprising the step of selectively removing said tunneling insulating film formed on the gate insulating film on the region where said MOS transistor is to be formed.

10. (Withdrawn) A method of manufacturing a semiconductor device according to claim 7, 8 or 9, wherein said oxidation-resistant film is a silicon nitride film.

11. (Canceled)

12. (Currently amended) The method of claim [[11]] 23 wherein the oxide film is formed by a single thermal oxidation step.

13. (Canceled)

14. (Currently amended) The method of claim [[13]] 24 wherein said oxidation-resistant layer is a silicon nitride layer.

15. (Currently amended) The method of claim [[13]] 24 wherein the oxide film is formed by a single thermal oxidation step.

16. (Canceled)

17. (Withdrawn) A semiconductor memory comprising:

a semiconductor substrate having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor formed on the semiconductor substrate,

wherein the oxide film on the floating gate of the non-volatile memory cell transistor and a gate insulating film of the MOS transistor are simultaneously and selectively formed in a single thermal oxidation step.

18. (Withdrawn) An apparatus comprising:

a semiconductor memory having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor formed on a semiconductor substrate,

wherein the oxide film on the floating gate of the non-volatile memory cell transistor and a gate insulating film of the MOS transistor are simultaneously and selectively formed in a single thermal oxidation step.

19. (Currently amended) The method of claim [[1]] 22, wherein the gate insulating film is approximately 150 nanometers thick.

20. (Currently amended) The method of claim [[11]] 23, wherein the gate insulating film is approximately 150 nanometers thick.

21. (Currently amended) The method of claim [[13]] 24, wherein the gate insulating film is approximately 150 nanometers thick.

22. (Currently amended) ~~The method of claim 1 comprising:~~

A method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate, said method comprising:

simultaneously and selectively forming the oxide film on the floating gate of the non-volatile memory cell transistor and a gate insulating film of the MOS transistor in a single thermal oxidation step;

forming a tunneling insulating film over the gate insulating film and the oxide film; and

selectively etching the tunnel insulating film on the region of the semiconductor substrate where the MOS transistor is to be formed.

23. (Currently amended) ~~The method of claim 11 comprising:~~

A method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate, said method comprising:

forming a silicon layer on the semiconductor substrate;

selectively removing the silicon layer on a region of the semiconductor substrate where the MOS transistor is to be formed;

forming an oxidation-resistant film over a first entire resulting surface;

selectively removing the oxidation-resistant layer on the region of the semiconductor substrate where the MOS transistor is to be formed and on a region of the semiconductor

substrate where the floating gate of the non-volatile memory cell transistor is to be formed;

simultaneously and selectively forming an oxide film on the region where the floating gate is to be formed and a gate insulating film on the region where the MOS transistor is to be formed;

forming a tunneling insulating film over the gate insulating film and the oxide film; and

selectively etching the tunnel insulating film on the region of the semiconductor substrate where the MOS transistor is to be formed.

24. (Currently amended) ~~The method of claim 13 comprising:~~

A method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on a same semiconductor substrate, said method comprising:

forming a gate insulating film on the semiconductor substrate;

forming a silicon layer on the gate insulating film;

selectively removing the silicon layer on a region of the semiconductor substrate where the MOS transistor is to be formed;

forming an oxidation-resistant film over a first entire resulting surface;

selectively removing the oxidation-resistant layer on the region of the semiconductor substrate where the high voltage MOS transistor is to be formed and on a region of the semiconductor substrate where the floating gate of the non-volatile memory cell transistor is to be formed;

simultaneously and selectively forming an oxide film on the region where the floating gate is to be formed and a gate insulating film on the region where the high voltage MOS transistor is to be formed;

removing at least some of the remaining oxidation-resistant film;

forming a tunnel insulating film over the gate insulating film and the oxide film; and

selectively etching the tunnel insulating film on the region of the semiconductor substrate where the MOS transistor is to be formed.

25. (New) The method of claim 22 including forming on the substrate a first MOS transistor for a first voltage and a second MOS transistor for a voltage higher than the first voltage, wherein during said selective etching of the tunnel insulating film, the tunnel insulating film is etched on the region where the first MOS transistor is to be formed.

26. (New) The method of claim 23 including forming on the substrate a first MOS transistor for a first voltage and a second MOS transistor for a voltage higher than the first voltage, wherein during said selective etching of the tunnel insulating film, the tunnel insulating film is etched on the region where the first MOS transistor is to be formed.

27. (New) The method of claim 24 including forming on the substrate a first MOS transistor for a first voltage and a second MOS transistor for a voltage higher than the first voltage, wherein during said selective etching of the tunnel insulating film, the tunnel insulating film is etched on the region where the first MOS transistor is to be formed.